TRANSISTOR PARAMETER EXTRACTION USING DC, S-PARAMETER AND NOISE DATA SIMULTANEOUSLY

Qian Cai, Jason Gerber, Tom Daniel and Ulrich L. Rohde

Compact Software, Inc.
201 McLean Blvd., Paterson, NJ, USA 07504

ABSTRACT

This paper presents, for the first time, an integrated method for transistor model parameter extraction by fitting the DC, multi-bias s-parameter and noise measurements simultaneously. The extracted model provides accurate small-signal, large-signal and noise characteristics. This technique is demonstrated for a Raytheon foundry HBT and excellent results are obtained. Self-heating effects are taken into consideration in the parameter extraction procedure.

INTRODUCTION

Low noise microwave circuit design engineers are often frustrated that the noise responses of the fabricated circuits are quite different from the results obtained using CAD programs. They may need several design passes to meet specifications. Even in mixer designs the noise of the fabricated circuits may be significantly higher than that predicted by the CAD tool. The discrepancy arises primarily from the poor estimation of the device noise figure.

Parameter extraction by fitting the model responses to measurements is the primary method to obtain the model parameter values of equivalent circuit models. Conventionally, parameter extraction is based on DC, s-parameter and large-signal measurements (e.g., [1]-[3]). The models extracted are suitable for DC, small- and large-signal analysis. However, noise analysis with these models often contains substantial errors.

This paper presents an integrated parameter extraction approach by fitting the model responses to the DC, multi-bias s-parameter and multi-bias noise measurements simultaneously. The models extracted not only provide precise characterization of device small- and large-signal responses but also give accurate prediction of device noise performance. The models can be used in a variety of applications for small- and large-signal as well as noise analysis. The advantages of our approach become more significant in the design of low noise microwave circuits.

Our method is demonstrated by parameter extraction for a Raytheon foundry heterojunction bipolar transistor (HBT). The model accounts for the device self-heating characteristics [4]. Two models are extracted: **Model 1** is based on DC and s-parameter measurements while **Model 2** is based on DC, s-parameter and noise measurements. Model 1 shows large errors in noise performance even though the DC and s-parameter fits are good. Model 2 provides accurate prediction in DC, s-parameter and noise responses. This technique is implemented in Compact Scout [5], a parameter extraction software tool, and the results are presented in this paper.

INTEGRATED PARAMETER EXTRACTION

The objective function for optimization in our integrated parameter extraction include DC, s-parameter and noise measurements. It is formulated as

$$\boldsymbol{E}_{total}(\phi) = \boldsymbol{E}_{DC}(\phi) + \boldsymbol{E}_{S}(\phi) + \boldsymbol{E}_{N}(\phi)$$

where ϕ are the model parameters to be extracted, $\boldsymbol{E}_{total}$ is the total error and

$$\boldsymbol{E}_{DC}(\phi) = \sum_{i=1}^{N_{DC}} \sum_{k,l}^{N_P} \| \boldsymbol{W}_{DC_{ikl}} [\boldsymbol{R}_{DC_{ikl}}(\phi) - \boldsymbol{M}_{DC_{ikl}}] \|$$

$$\boldsymbol{E}_{S}(\phi) = \sum_{i=1}^{N_{SDC}} \sum_{j=1}^{N_{SF}} \sum_{k,l}^{N_P} \| \boldsymbol{W}_{S_{ijkl}} [\boldsymbol{R}_{S_{ijkl}}(\phi) - \boldsymbol{M}_{S_{ijkl}}] \|$$

$$\boldsymbol{E}_{N}(\phi) = \sum_{i=1}^{N_{NDC}} \sum_{j=1}^{N_{NF}} \sum_{k}^{N_{NP}} \| \boldsymbol{W}_{N_{ijk}} [\boldsymbol{R}_{N_{ijk}}(\phi) - \boldsymbol{M}_{N_{ijk}}] \|$$

are the DC error, s-parameter error and noise error, respectively. N_P is the number of ports of the device. N_{DC} is the number of DC measurement points. N_{SDC} and N_{SF} are, respectively, the number of bias points and frequencies at which the s-parameter measurements are taken. N_{NP} is the number of noise parameters and N_{NDC} and N_{NF} are, respectively, the number of bias points and frequencies at which the noise measurements are taken. The ***R***'s and ***M***'s are the model responses and the corresponding

0-7803-4603-6/97/$5.00 (c) IEEE

measurements. The $\boldsymbol{W}$'s are the weighting factors applied to the corresponding errors. The ||•|| denotes the least-squares norm. A Levenberg-Marquardt optimization process was applied to:

$$\underset{\phi}{\text{minimize}} \quad \boldsymbol{E}_{total}(\phi)$$

The DC, multi-bias s-parameter and multi-bias noise measurements are simultaneously matched to the model response during optimization. A direct parameter extraction and level by level optimization strategy [5] can be used for efficient model extraction.

DEVICE SIMULATION AND NOISE CALCULATION

The device model used in our parameter extraction consists of three parts: intrinsic circuit, device parasitics and package parasitics as shown in Fig. 1. The DC bias point is first obtained by DC simulation. A small-signal equivalent circuit is then established by linearizing the model at the bias point and this is used for s-parameter and noise calculations. The small-signal model (including the intrinsic and extrinsic circuits for BJTs and HBTs) is shown in Fig. 2.

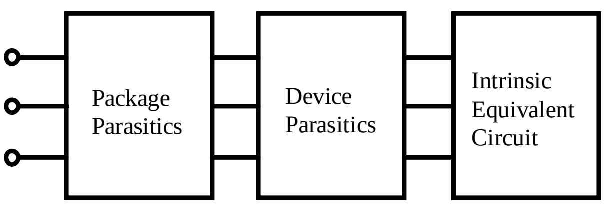


Fig. 1 Three parts of equivalent circuit for device model.

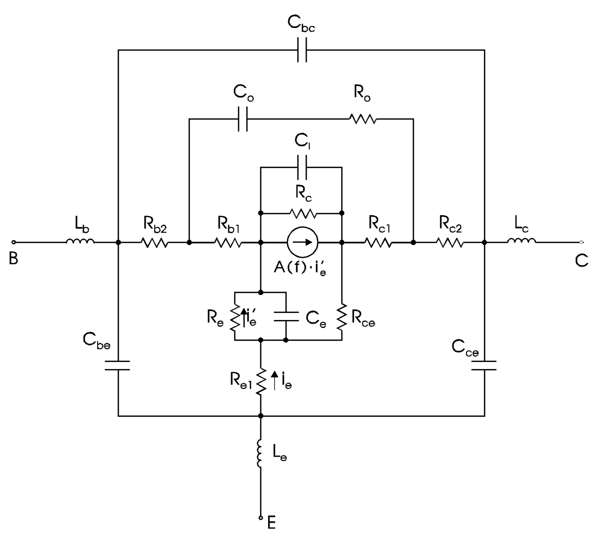


Fig. 2 The small-signal equivalent circuit including the intrinsic and extrinsic parts for BJTs and HBTs. The collector-emitter resistor Rce is important in parameter extraction.

For the noise responses, the minimum noise figure $\boldsymbol{F}_{min}$, the optimal noise reflection coefficient Γ_{opt} and the equivalent normalized noise resistance $\boldsymbol{R}_N$ are calculated. For the circuit shown in Fig. 2, the intrinsic noise parameters are evaluated using the following equations [6,7].

$$\boldsymbol{F}_{Min} = \boldsymbol{a}\frac{\boldsymbol{R}_{b1} + \boldsymbol{R}_{opt}}{\boldsymbol{R}_e} + \left(1 + \frac{\boldsymbol{f}^2}{\boldsymbol{f}_b^2}\right)\frac{1}{\boldsymbol{A}_0} + \frac{\boldsymbol{F}_C}{1 + \boldsymbol{f}}$$

The optimum source resistance is calculated by

$$\boldsymbol{R}_{opt} = \left[\boldsymbol{R}_{b1}^2 - \boldsymbol{X}_{opt}^2 + \left(1 + \frac{\boldsymbol{f}^2}{\boldsymbol{f}_b^2}\right)\frac{\boldsymbol{R}_e(2\boldsymbol{R}_{b1} + \boldsymbol{R}_e)}{\boldsymbol{A}_0\boldsymbol{a}}\right]^{1/2}$$

the optimum source reactance is

$$\boldsymbol{X}_{opt} = \left(1 + \frac{\boldsymbol{f}^2}{\boldsymbol{f}_b^2}\right)\frac{2\pi\boldsymbol{f}\boldsymbol{C}_e\boldsymbol{R}_e^2}{\boldsymbol{A}_0\boldsymbol{a}}$$

and the normalized noise resistance is

$$\boldsymbol{R}_N = \boldsymbol{R}_{b1}\left(\boldsymbol{A} + 1 - \frac{1}{\boldsymbol{A}_0}\right) + \frac{\boldsymbol{R}_e}{2}\left[\boldsymbol{A} + \frac{\boldsymbol{R}_{b1}^2}{\boldsymbol{R}_e^2}\left(1 + \frac{\boldsymbol{f}^2}{\boldsymbol{f}_b^2} - \boldsymbol{A}_0 + \frac{\boldsymbol{f}^2}{\boldsymbol{f}_e^2}\right)\right]$$

where $\boldsymbol{f}$ is the operating frequency, $\boldsymbol{f}_b$ is the cutoff frequency of the common base current gain $\boldsymbol{A}(\boldsymbol{f})$, $\boldsymbol{A}_0$ is the DC current gain, $\boldsymbol{T}_j$ is the device temperature and F_C is the Flicker noise corner frequency. The coefficients $\boldsymbol{a}$ and $\boldsymbol{f}_e$ are calculated as follows.

$$\boldsymbol{a} = \left[\left(1 + \frac{\boldsymbol{f}^2}{\boldsymbol{f}_b^2}\right)\left(1 + \frac{\boldsymbol{f}^2}{\boldsymbol{f}_b^2}\right) - \boldsymbol{A}_0\right]\frac{1}{\boldsymbol{A}_0}$$

$$\boldsymbol{f}_e = \frac{1}{2\pi\boldsymbol{N}_{fac}\boldsymbol{C}_e\boldsymbol{R}_e^2}$$

where $\boldsymbol{N}_{fac}$ is a noise factor. The effect of the device and package parasitic circuits are included in the calculation of the total device noise.

PARAMETER EXTRACTION OF A HBT MODEL

Parameter extraction of a HBT model [4] is carried out to demonstrate the features of our integrated method. The device self-heating effects are modeled by a thermal circuit. The model equation can be generally written as

$$\boldsymbol{V}_{BE} = \boldsymbol{V}_{BE}\left(\phi, \boldsymbol{I}_B, \boldsymbol{V}_{CE}, \boldsymbol{T}_j(\phi, \boldsymbol{I}_B, \boldsymbol{V}_{CE})\right)$$

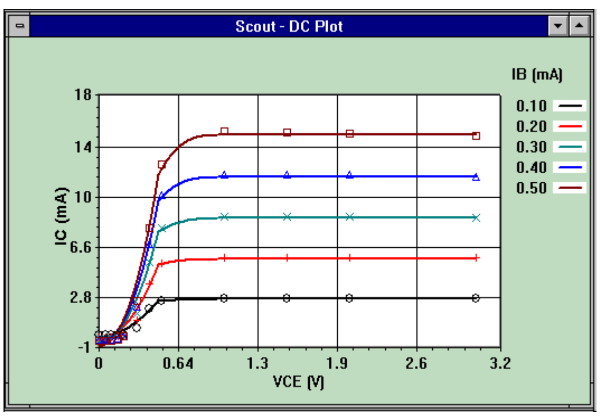
$$\boldsymbol{I}_C = \boldsymbol{I}_C\left(\phi, \boldsymbol{I}_B, \boldsymbol{V}_{CE}, \boldsymbol{T}_j(\phi, \boldsymbol{I}_B, \boldsymbol{V}_{CE})\right)$$

which indicate that $\boldsymbol{V}_{BE}$ and $\boldsymbol{I}_C$ are functions of model parameters ϕ, bias point ($\boldsymbol{I}_B$, $\boldsymbol{V}_{CE}$) and temperature $\boldsymbol{T}_j$. The

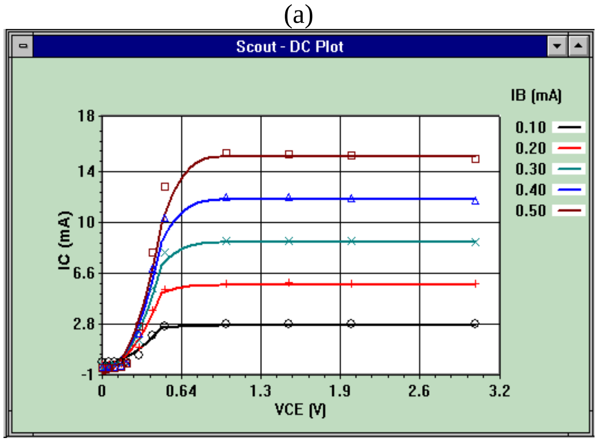
0-7803-4603-6/97/$5.00 (c) IEEE

device temperature is also depend on the model parameters and bias conditions.

The data used for parameter extraction include DC measurements at 60 points, s-parameter measurements and noise measurements at 9 bias points and 17 frequencies. Two models are extracted: Model 1 using DC and s-parameter measurements while Model 2 using DC, s-parameter and **noise measurements**. The most significant difference between Model 1 and Model 2 are the values of those parameters which affect the device noise responses such as R_{b1}, R_e and C_e, etc. The modeled and measured DC responses are plotted in Fig. 3. The modeled and measured S parameters at two bias points are shown in Figs. 4-5. The modeled and measured minimum noise figures at two bias points are shown in Figs. 6-7. From Figs. 3-5 we can see that the DC responses and s parameters of both models match the measurements very well. However, the noise responses of Model 2 are much closer to the measurements than those of Model 1 which are illustrated in Figs. 6-7. If both models are used for noise analysis in circuit design, Model 2 will provide much more accurate results than Model 1.

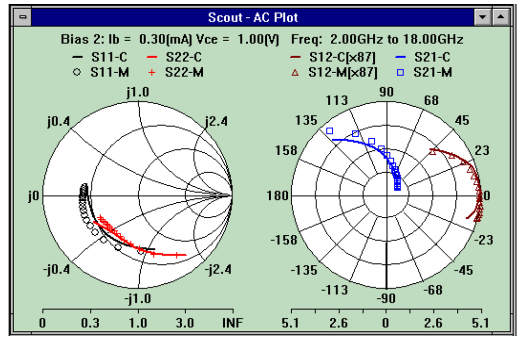


(a)

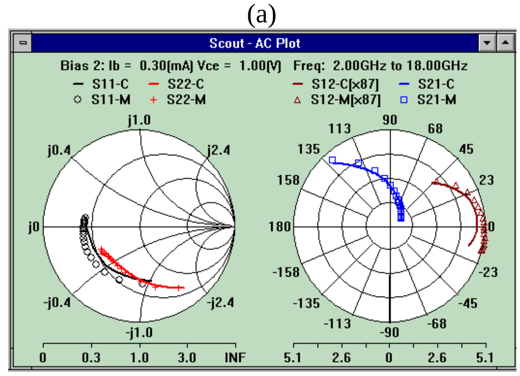


(b)

Fig. 3 Measured (discrete points) and modeled (solid lines) DC I-V curves of (a) Model 1 and (b) Model 2.

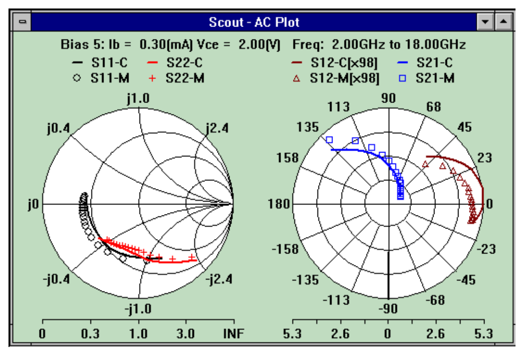


(a)

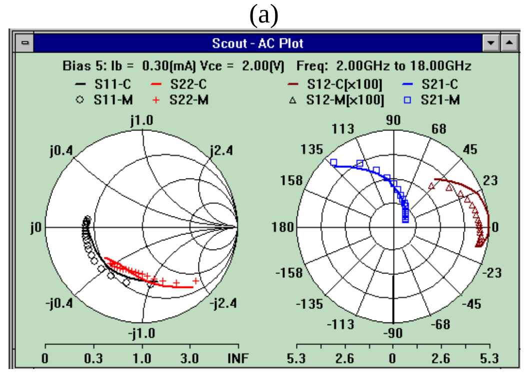


(b)

Fig. 4 Measured (discrete points) and modeled (solid lines) S parameters of (a) Model 1 and (b) Model 2 at bias point Ib = 0.3mA and Vce = 1V.

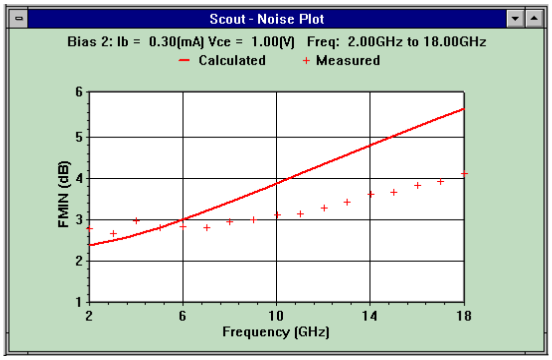


(a)

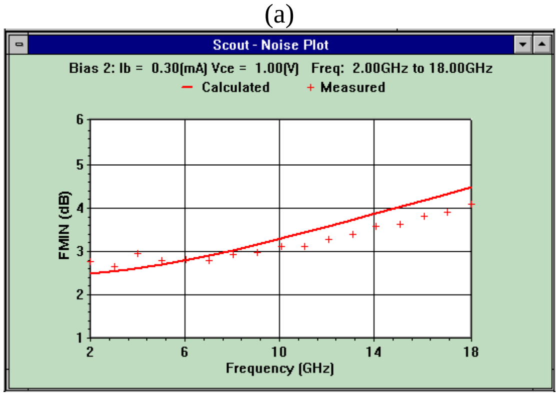


(b)

Fig. 5 Measured (discrete points) and modeled (solid lines) S parameters of (a) Model 1 and (b) Model 2 at bias point Ib = 0.3mA and Vce = 2V.

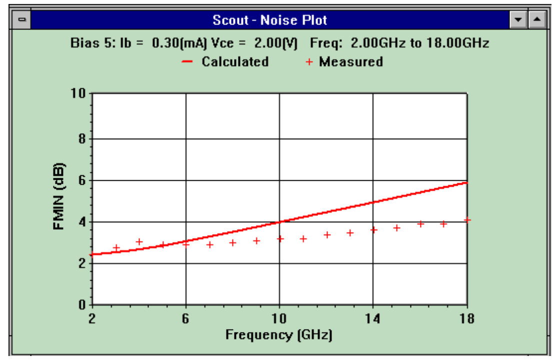


(a)

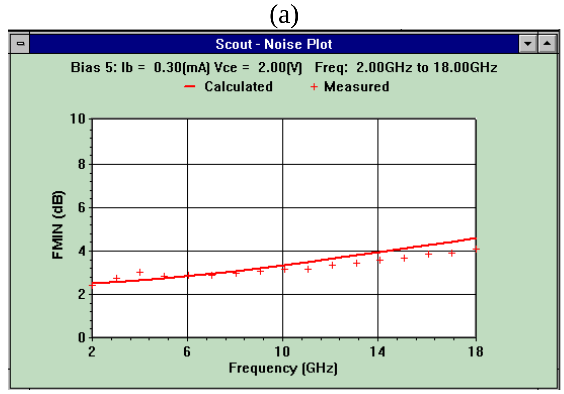


(b)

Fig. 6 Measured (discrete points) and modeled (solid lines) minimum noise figures of (a) Model 1 and (b) Model 2 at bias point Ib = 0.3mA and Vce = 1V.



(a)



(b)

Fig. 7 Measured (discrete points) and modeled (solid lines) minimum noise figures of (a) Model 1 and (b) Model 2 at bias point Ib = 0.3mA and Vce = 2V.

CONCLUSIONS

We have presented an integrated parameter extraction method fitting DC, multi-bias s-parameter and multi-bias noise measurements simultaneously. The models extracted using this approach are capable of predicting the device small- and large-signal as well as noise performances accurately and can be used in a wide range of applications. Microwave circuit design engineers will benefit from such models to attain first-pass circuit design and thus reduce the development cost.

ACKNOWLEDGMENT

This work was sponsored, in part, by the Air Force Phase II SBIR Program on Bias-Dependent Noise Modeling of HBTs. The authors would like to thank Bob Neidhard of WL/ELM, Wright Patterson Air Force Base for providing measurements and Raytheon Co. for supplying the HBT device.

REFERENCES

[1] J.W. Bandler, R.M. Biernacki, Q. Cai, S.H. Chen, S. Ye and Q.J. Zhang, "Integrated physics-oriented statistical modeling, simulation and optimization," *IEEE Trans. Microwave Theory Tech.*, vol. 40, pp. 1374-1400, 1992.

[2] S.G. Skaggs, J. Gerber, G. Bilbro and M.B. Steer, "Parameter extraction of microwave transistors using a hybrid gradient descent and tree annealing approach," *IEEE Trans. Microwave Theory Tech.*, vol. 41, pp. 726-729, 1993.

[3] T. Fernández, Y. Newport, J.M. Zamanillo, A. Tazón, and A. Mediavilla, "Extracting a bias-dependent large-signal MESFET model from pulsed I/V measurements," *IEEE Trans. Microwave Theory Tech.*, vol. 44, pp. 372-378, 1996.

[4] R. Anholt, J. Gerber, R. Tayrani and J. Pence, "HBT model parameter extractor for SPICE and harmonic balance simulators," *IEEE MTT-S Int. Microwave Symp. Digest*, pp. 1257-1260, 1994.

[5] *Compact Scout Reference Manual*, Compact Software, Inc., Paterson, NJ.

[6] U.L. Rohde and C.R. Chang, "Parameter extraction for large-signal noise models and simulation of noise in large-signal circuits," *Microwave Journal*, pp. 222-239, May, 1993.

[7] R.A. Pucel and U.L. Rohde, "An accurate expression for the noise resistance Rn of a bipolar transistor for use with the Hawkins noise model," *IEEE Microwave and Guided Wave Letters*, Vol. 3, pp. 35-37, 1993.